Research on the Experimental Teaching Reform of Computer Organization Principles Based on Proteus Virtual Simulation

Zhiyuan Sun, Kaile Xiao*, Jianguo Liu, Leizhen Ma
Beijing Union University, Beijing 100101, China

Abstract: In view of the problems such as hardware solidification, cumbersome operation and poor flexibility existing in the traditional experimental teaching of computer organization principles, this study proposes an experimental teaching reform plan based on Proteus virtual simulation. A complete virtual simulation experimental teaching system has been established by constructing hierarchical experimental modules. During the implementation of the reform, four steps were adopted: theoretical preparation, simulation tool training, hierarchical experiments, and innovative challenges, to ensure that students could gradually master the design and implementation methods of computer hardware systems. After two semesters of teaching practice, the results show that the students' experimental completion rate has increased from 68% to 92%, the accuracy rate of knowledge point mastery has risen by 46%, 85% of the students believe that virtual simulation is more intuitive than traditional experiments, and 70% of the students indicate that their innovation ability has been significantly enhanced. This study also constructed a complete teaching resource system including a virtual experiment library, supporting teaching materials and teaching papers. In the future, the experimental scenarios will be further expanded, with the addition of contents such as the collaborative design of Cache and main memory, and the simulation of multi-core CPU storage consistency. A hybrid experimental platform of "virtual simulation +FPGA verification" will also be constructed to continuously improve the quality and effect of the experimental teaching of computer organization principles.
***Keywords*:** Proteus virtual simulation, principles of computer organization, experimental teaching reform, hierarchical experimental design, cultivation of innovation ability

1. Introduction

Principles of Computer Organization, a core foundational course for the Computer Science and Technology major, is highly theoretical and abstract [1]. Incorporating experiments is crucial for aiding student comprehension. In traditional experimental teaching, hands-on practice primarily relies on physical experiment kits[2-3]. However, this approach suffers from significant drawbacks, including fixed hardware configurations, cumbersome procedures, and limited flexibility. Students are often confined to connecting pre-set wires following a rigid sequence, unable to independently design the architectural connection between the CPU and memory. This severely constrains the development of their innovative capabilities. Furthermore, physical experiment kits are expensive, incur high maintenance costs, and experimental results are easily affected by various interfering factors, making it difficult to meet the demands of large-scale teaching.

In recent years, advancements in information technology have provided a new solution for experimental teaching in this field: virtual simulation technology[4]. Xiong Taiping et al. noted that for students majoring in Software Engineering, Information Security, and related fields, their typically weaker foundation in hardware description language programming, combined with factors like reduced course hours, significantly diminishes the effectiveness of traditional experimental methods [5]. Wu Yan et al. emphasized that a hierarchical simulation experiment design, tailored to the needs of different majors, can effectively enhance teaching outcomes [6]. The experimental teaching system that combines virtual and real elements has been verified to play a positive role in consolidating students' basic knowledge and enhancing their practical abilities [7-8].

Building on this foundation, this study proposes a curriculum reform plan centered on Proteus virtual simulation. Grounded in constructivist learning theory and the concept of stratified teaching, it emphasizes students' active construction of knowledge through practical activities. The virtual simulation environment provides a safe space for students to explore independently. The stratified teaching concept is implemented through the design of differentiated experimental content, catering to varying professional backgrounds and student ability levels.

2. Teaching Design

2.1 Experimental Module Design

Guided by the principles of stratified teaching and professional demand orientation, this research uses the CPU-memory connection as an example to design progressive experimental modules. Each module is closely aligned with the core knowledge points of the Principles of Computer Organization and thoroughly considers the cultivation of students' system design capabilities, as illustrated in Table 1.

Table 1. Design of the CPU and Memory Connection Experiment Module

Experimental Module	Knowledge Involved	Ability Cultivated	Proteus Correlation
Single-Chip Connection	Address line allocation, chip select signal logic, basic read/write functions	Basic hardware cognition	Use Proteus to draw address and data lines between an 8×8-bit memory chip and the CPU, verifying basic read/write operations.
Bit Expansion & Word Expansion Simulation	Multi-chip bit/word expansion, decoder (e.g., 74LS138) configuration, address space division	Circuit design	Simulate bit expansion (e.g., eight 8K×1-bit chips forming an 8K×8-bit memory) and word expansion using decoder-based chip selection.
Combined Word & Bit Expansion Design	Building a composite memory system, high-order address decoding, chip select logic optimization	System integration	Construct a 64K×8-bit storage system from 16K×4-bit chips via bit and word expansion, integrating a decoder for chip select control.
Address Space Allocation Based on Real Cases	Address decoding, chip select logic gate circuit design, memory space partitioning for different purposes (e.g., system/user program areas)	Engineering application	Design address decoding and chip select logic for a practical scenario (e.g., a 16-bit CPU with 8-bit data lines), allocating address space for system and user program areas.
Advanced Scalability: Pipelined CPU	Pipelined CPU architecture, memory interaction timing, performance optimization, pipeline hazard resolution, memory bandwidth optimization	Innovative design	Build a pipelined CPU architecture in Proteus, simulate its interaction timing with memory, and analyze performance optimization and conflict resolution.

In the single-chip connection module, students are required to master the principles of address line connection and the methods for generating chip select signals. Using Proteus's signal generator to simulate CPU read/write operations, they observe the data values transmitted on the data bus and verify the basic functionality of the memory chip. Moving to the bit expansion and word expansion modules, the focus shifts to training students in understanding and applying the working principles of decoders. For example, the 74LS138 decoder is utilized to implement chip selection control for multiple memory chips, helping students grasp the methods and logic behind address space partitioning. In the combined word-bit expansion module, students are expected to comprehensively apply knowledge from the previous modules to solve practical memory design problems. A typical task involves designing a memory system that meets specific capacity requirements using memory chips of different specifications, while also optimizing the address decoding circuit. Finally, in the advanced expansion module, the pipelined CPU design is introduced. This module enables students to understand how modern processors use pipelining to enhance performance, as well as the types of pipeline conflicts that arise and their corresponding solutions.

2.2 Implementation Steps

To ensure the smooth execution of the reform plan, the following four implementation steps have been designed:

(1) Theoretical Preparation: Before the experiments begin, instructors will systematically explain the principles of memory expansion (including bit, word, and combined word-bit expansion), the working mechanism of decoders (such as the 74LS138), and methods for address space division. Emphasis will be placed on the fundamental principles of address decoding circuit design, including the advantages, disadvantages, and applicable scenarios of full decoding, partial decoding, and linear selection methods.

(2) Simulation Tool Training: Students will be guided to master basic Proteus operations, including circuit diagram drafting, signal debugging (e.g., address line stability analysis), and related techniques. Through demonstrations of typical cases, students will become familiar with debugging methods in a virtual simulation environment—such as using a logic analyzer to observe timing waveforms and setting breakpoints to identify and resolve circuit design errors.

(3) Stratified Experimentation: A progressive experimental structure is adopted to accommodate the learning needs of students at different levels. The basic tier focuses on single-chip connection and read-write verification; the advanced tier involves multi-chip expansion and decoder design; and the comprehensive tier requires complex address space allocation tasks.

(4) Innovation Challenge: Students are encouraged to design non-standard expansion schemes—such as hybrid

approaches combining linear selection with decoder-based methods—and to compare performance differences. This phase aims to cultivate innovative thinking and engineering optimization capabilities.

3. Analysis of Reform Achievements

3.1 Teaching Achievements

Through two semesters of teaching practice, the virtual simulation reform has achieved remarkable results in enhancing students' abilities and cultivating innovative projects.

In terms of students' abilities, after the reform, students generally mastered the hardware design methods for connecting memory and CPU (such as address decoding and chip selection logic). Experimental reports show that the accuracy rate of key knowledge points has increased by more than 30%. Students can independently solve problems such as address conflicts and data bus contention (for example, optimizing signal stability through timing simulation). More importantly, students have shown remarkable progress in system design ability and problem analysis ability.

In terms of innovative projects, the student team designed several creative memory systems, such as a hybrid decoding scheme with bit expansion and a multi-body memory with low-bit cross-addressing, and verified their feasibility through Proteus simulation. These projects not only deepened students' understanding of the principles of computer organization, but also laid a foundation for subsequent course studies and scientific research activities.

3.2 Resource Construction

To support virtual simulation teaching, Proteus simulation templates for the Computer Organization Principles course experiments (such as line selection method, decoder chip selection method, and pipeline CPU) were constructed, covering the core knowledge points of "Computer Organization Principles". The experimental library adopts a modular design, allowing teachers to flexibly combine experimental content according to teaching needs.

Supplementary textbook: Authored "Virtual Experiment Guide for Principles of Computer Organization", which provides a detailed analysis of the experimental design ideas and simulation steps. The teaching materials are written in a problem-oriented manner, guiding students to master the thinking methods of hardware design through practical cases.

Teaching paper: A reform paper on the virtual simulation experiment design of computer organization principles was formed, systematically summarizing the reform experience and achievements, providing a reference for the teaching reform of similar institutions.

4. Teaching effectiveness evaluation

To comprehensively evaluate the reform effect, multiple assessment methods were adopted, including quantitative indicators such as the completion degree of experiments, the innovativeness of circuit design, and the accuracy of simulation results, as well as qualitative evaluations such as student feedback surveys.

Through the follow-up assessment of two batches of students, it was found that the virtual simulation experiment significantly improved the students' learning experience and the quality of their outcomes. The specific assessment results are shown in Table 2 below.

Table 2. A comparison of students' performance before and after teaching reform

Evaluation Metrics	Pre-reform (Traditional Experiments)	Post-reform (Virtual Simulation)	Improvement
Experiment Completion Rate	68%	92%	35%
Circuit Design Innovation	Mainly basic function implementation	Diversified design solutions emerged	Significant
Knowledge Mastery Accuracy	58%	85%	46%
Willingness for Self-directed Experiments	Moderate	High	Significant
Complex Problem-Solving Ability	Relatively weak	Markedly enhanced	Significant

5. Conclusion

This study addresses the limitations of traditional experimental teaching in the Principles of Computer Organization by proposing a teaching reform plan centered on Proteus virtual simulation. Through systematic experimental module design and a hierarchical implementation approach, students' practical abilities, innovative thinking, and system design capabilities have been significantly enhanced. Reform practice has demonstrated that virtual simulation not only reduces experimental costs but also expands the depth and breadth of experimental content, enabling the implementation of advanced experiments that were difficult to conduct in traditional environments.

In the future, AI-assisted debugging capabilities will be introduced, and an intelligent diagnostic system will be developed to automatically identify circuit design errors and provide targeted improvement suggestions. This function will greatly alleviate the guidance burden on instructors while offering students immediate feedback to enhance learning outcomes. Experimental scenarios will be further expanded to expose students to cutting-edge technologies in modern computer architecture, laying a foundation for their subsequent learning and research. A hybrid experimental platform will also be established by integrating Proteus virtual simulation with FPGA physical verification, forming a dual-track experimental model of "virtual design + physical verification." Students will first complete design optimization in a virtual environment and then conduct physical verification through the FPGA platform, experiencing the complete hardware development process.

Overall, the reform of virtual simulation experiment teaching represents not only a technological upgrade of experimental methods but also a profound transformation of teaching philosophy. By creating an open, safe, and exploratory learning environment, it stimulates students' creative potential, cultivates their computational thinking and system capabilities, and lays a solid foundation for addressing the challenges of the artificial intelligence era.

Acknowledgments

This paper is supported by R&D Program of Beijing Municipal Education Commission (KM202311417003, KM202311417004) and the Academic Research Projects of Beijing Union University (No. ZK20202205, No. ZK20202214).

References

[1] Zheng, F., Wang, Q., and Xu, J. (2023). Research on the Experimental Teaching Model of Computer Composition Principles Based on Virtual Simulation Technology. China Education Info, vol. 29, no. 5, pp. 88-92.

[2] Zhang, D., Cheng, X., Gao, Z., et al. (2024). Experiment Teaching Case Design of Computer I/O Channel Virtual Simulation. In: Proceedings of the International Conference on Education. Singapore: Springer Nature, pp. 89-102.

[3] Cai, X., Fan, Y. R., Li, G., etc. (2022). Design and Discussion on Virtual Simulation of Instruction Execution in von Neumann Computer. Experimental Technology and Management, vol. 39, no. 5, pp. 89-93.

[4] Dai, L. and Zhu, H. (2023). Research on the Construction of a Virtual Simulation 'Golden Course': Taking Computer Composition Principles as an Example. Experimental Science and Technology, vol. 21, no. 2, pp. 78-82.

[5] Xiong, T. P., Chen, H., and Guan, J. L. (2024). Utilizing Logisim and Head Song to Reconstruct the Experimental Teaching of Computer Composition Principles. Computer Knowledge and Technology, vol. 20, no. 18, pp. 156-159.

[6] Wu, Y., Gao, Z., Wang, Q. Y., etc. (2024). Research on the Design of Computer Composition Principle Simulation Experiments Oriented to Professional Needs. Computer Knowledge and Technology, vol. 20, no. 14, pp. 102-105.

[7] Tan, Z. H. (2023). Construction of an Online Practical Teaching System for Computer Composition Principles Based on LOGISIM. In: National Conference on Computer Education in Universities, Proceedings of the 2023 Computer Education Conference. Beijing: Tsinghua University Press, pp. 45-49.

[8] Wang, S. and Liu, R. (2024). Research on Virtual Simulation Experiment Teaching of Computer Composition Principles under the Background of Emerging Engineering Education. Higher Engineering Education Research, vol. 42, no. 1, pp. 135-140.